B1

6. (New) The electronic phase-locked loop as claimed in claim 5, wherein the PI filter has an integral regulation, a linear regulation and an addition and amplifier stage, which is driven by the analog phase detector via a line.--

REMARKS

In the above-identified application, claims 1 and 2 have been objected to because of certain stated informalities while claims 1-4 were rejected as being indefinite. Applicants have canceled claims 1-4 and hereby submit claims 5 and 6 which should obviate all of the objections and indefiniteness rejections herein.

In addition, the Examiner has rejected claims 1, 3 and 4 as being anticipated by U.S. patent No. 6,028,460 to McCollum et al. Claim 2 has been rejected as being obvious over the same patent to McCollum et al. The Examiner has stated that it would have been obvious to implement McCollum's divider 340 using flip-flops functioning as a counter.

As set forth above, Applicants have resubmitted the claims as new claims 5 and 6 and, as resubmitted, believes they now distinguish over McCollum et al.

More particularly, McCollum et al. describe a multi-frequency synthesizer containing an analog PLL 200, a digital PLL 300 and a PLL control unit 400 for controlling the switching of the synthesizer between a digital mode of the digital PLL 300 and an analog mode of the analog PLL 200. The digital PLL 300 provides an accelerated and accurate frequency acquisition mode, whereas the analog PLL 200 provides an operation mode, after the frequency has been "locked". The switching between analog and digital PLL is being done by means of the controllable switch 500. This controllable switch 500 is controlled via the output signal of control circuit 400.

McCollum et al. does not describe or suggest a lock detection circuit. In McCollum et al. the control circuit only monitors whether the frequency is locked or not. McCollum et al. does not disclose the functionality of the lock detection circuit as now claimed; the subject invention activates the analog PLL for the controlling of the oscillator in a continuously variable manner depending on the counter reading of a discrete operating counter. According to the subject

invention the lock detection circuit deactivates the analog PLL if the phase error between the output clock signal and the reference clock signal exceeds a specific phase error. Neither this activating functionality nor the deactivating functionality is disclosed in McCollum et al. Moreover, McCollum et al. fail to disclose that the analog phase detector is activated to avoid a phase quantization error if the counter reading of the counter is zero and is being deactivated again if the counter reading of the counter exceeds a specific phase error value.

McCollum et al. also fail to disclose a digitally controllable oscillator of the PLL which receives a digital control signal of the drive circuit. McCollum et al. only disclose a voltage controlled oscillator 240 which is being controlled by an analog voltage signal coupled in from the loop filter 230.

Finally, the objects of the present invention and McCollum et al. are different. It is the object of the present invention to attenuate jitters on the lowest possible digital discrete level of the counter. The object of McCollum et al. is however to provide a multi-frequency synthesizer with enhanced control (see column 2, lines 42ff).

Applicants hereby request reconsideration and reexamination thereof.

With the above amendments and remarks, this application is considered ready for allowance and Applicants earnestly solicit an early notice of same. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned at the below-listed number.

Respectfully submitted,

WELSH & KATZ, LTD.

Gerald T. Shekleton

Gerald T. Shekleton
Registration No. 27,466

Date: March 18, 2003
WELSH & KATZ, LTD.
120 South Riverside Plaza
22nd Floor
Chicago, Illinois 60606-3913
Telephone: 312/655-1500